CLAIMS

1. A pixel cell in an active matrix OLED display, comprising:

an OLED, the OLED having an anode and a cathode, the anode coupled to a common reference line;

a current supply line, the OLED cathode coupled to the current supply line; and

a plurality of static cells, each static cell comprising:

a memory element, the memory element having a bitline input, a power input, a select input, and a data output, the bitline input coupled to at least one bit of a column data line of the active matrix OLED display, the power input coupled to a reference voltage source, the select input coupled to a row select line of the active matrix OLED display; and

a current driver, the current driver having an output current level proportional to the bit position of the column data line bit coupled to the bitline input of the memory element, the current driver also having a control input, a supply voltage input, and a current output, the control input coupled to the data output of the memory element, the supply voltage input coupled to a supply voltage source, the current output coupled to the current supply line.

2. The pixel cell of Claim 1, wherein the output current of the current driver of a static cell is proportional to the bit position of the column data line bit coupled to the bitline input of the memory element as provided by the relationship:

$$I_{out} = I_{base} * 2^n$$

Where:

I_{out} is output current of the current driver,

I_{base} is the interval current unit for the grayscale step, and

n is the bit position of the output bit that is provided to the current driver from the memory element.

3. The pixel cell of Claim 1, wherein the memory element of each static cell comprises a pair of cross-coupled inverters and an access transistor.
4. The pixel cell of Claim 3, wherein the cross-coupled inverters are formed by cross coupled MOS transistor pairs and the access transistor is a MOS transistor.
5. The pixel cell of Claim 4, wherein the access transistor drain is coupled to a true port of the cross-coupled inverters and the current driver control input is coupled to a complement port of the cross-coupled inverters.
6. The pixel cell of Claim 1, wherein the current driver is a MOS transistor.
7. The pixel cell of Claim 6, wherein the current driver is a P-type MOS transistor.
8. A method for controlling the grayscale current provided to an OLED in an active matrix display, comprising:

storing digital data corresponding to pixel grayscale in a plurality of static memory elements of the display, each element storing at least one data bit;

providing a plurality of current drivers, each current driver corresponding to a data bit which is stored in one of said plurality of memory elements, the output current from each current driver provided to a common current supply line which is coupled to the OLED; and

delivering each data bit to a control input of the corresponding current driver to control the grayscale current provided to the OLED.

9. A pixel cell for use in an active matrix display, comprising:

a plurality of static memory elements, each having a data input, a select input, a power input, and a control signal output for supplying first and second control signals for activating and deactivating a current driver, respectively; and

current drivers associated with said memory element, wherein each current driver has an output connected to a common signal line, a control signal input connected to the control signal output of its associated memory element, and a power input, wherein said current drivers include a first current driver and a second current driver, the first current driver, responsive to receiving a first control signal, outputs a first predetermined current, and the second current driver, responsive to receiving a first control signal, outputs a second predetermined current which is different from said first predetermined current.

10. A pixel cell according to claim 9, wherein a third current driver, responsive to receiving a first control signal, outputs a third predetermined current which is different from said first and second predetermined currents.

11. The pixel cell of Claim 9, wherein the predetermined current of each current driver is proportional to the bit position of a column data line bit coupled to the data input of an associated memory element as provided by the relationship:

$$I_{out} = I_{base} * 2^n$$

Where:

I_{out} is the predetermined current of the current driver,

I_{base} is the interval current unit for the grayscale step, and

n is the bit position of the control signal output that is provided to the current driver from the associated memory element.

12. The pixel cell of Claim 9, wherein the memory element comprises a pair of cross-coupled inverters and an access transistor.

13. The pixel cell of Claim 12, wherein the cross-coupled inverters are formed by cross coupled MOS transistor pairs and the access transistor is a MOS transistor.

14. The pixel cell of Claim 13, wherein the access transistor drain is coupled to a true port of the cross-coupled inverters and the current driver control input is coupled to a complement port of the cross-coupled inverters.

15. The pixel cell of Claim 9, wherein each current driver is a MOS transistor.

16. The pixel cell of Claim 15, wherein each current driver is a P-type MOS transistor.